WHAT IS CLAIMED:

1. A method for increasing the number of real memory addresses accessible through a translation look aside buffer (TLB) by a multi thread CPU comprising:

storing in said buffer entries including a virtual address, a real address and a special mode bit indicating whether said address represents one of a plurality of threads being processed;

concatenating to higher order bits of said real address a value representing a thread being processed when said buffer entries are read by a processor in which said special mode bit indicates a thread is being processed; and

concatenating to said real address the lower order bits of said real address when said special mode bit indicates a thread is not being processed.

2. The method according to claim 1 wherein said virtual address defines a plurality of pages in a memory, and said value representing said thread identifies a page within said plurality of pages when said special mode bit is set.

3. The method according to claim 1 wherein said virtual address comprises an effective address and a process identifier unique to each process requiring data located at said real address.

4. The method according to claim 1 wherein said lower order bits of said concatenated real address identify a page in a group of pages stored in a memory.

5. The method according to claim 1 wherein said real address stored in said buffer constitutes the higher order bits of an address in said real memory.

6. A method for increasing the number of real memory addresses accessible through a translation look aside buffer (TLB) by a multi thread CPU comprising:

storing in said buffer entries including a virtual address, a real address and a special mode bit indicating whether said address represents one of a plurality of threads being processed;

concatenating to higher order bits of said real address a value representing a thread being processed when said buffer entries are read by a processor in which said special mode bit indicates a thread is being processed;

concatenating to said real address the lower order bits of said real address when said special mode bit indicates a thread is not being processed; and

further concatenating a portion of said virtual address to said concatenated real address.

7. The method for increasing the number of real memory addresses accessible through a translation look aside buffer according to claim 6 wherein said virtual address comprises an effective address and a process identification number.

8. The method for increasing the number of real memory addresses accessible through a translation look aside buffer according to claim 7 wherein said portion of said virtual address which is concatenated with said real address includes the lower order bits of said effective address.

9. A translation look aside buffer for identifying real addresses of data stored in a memory for a plurality of threads being executed by a multi-thread CPU comprising:

an array of storage elements which caches address translation key value pairs;

a search engine for searching said translation key pairs to locate a real address of a group of pages stored in memory which are identified by a virtual page address, and a thread implicit mode bit associated with said virtual address;

a first logic circuit connected to receive said thread implicit bit; and concatenating with said real address of said group of pages data bits representing a thread being processed by said multithread CPU when said thread implicit bit is set to a first value.

10. The translation look aside buffer according to claim 9 wherein said logic circuit concatenates lower order bits derived from said real address to said address of said group of pages when said thread implicit bit is set to a second value.

11. The translation look aside buffer according to claim 10 wherein said real address bits are further concatenated with the lower order bits of said virtual address.

12. The translation look aside buffer according to claim 9 wherein said virtual address is derived from a process number and an effective address provided by said CPU.

13. The translation look aside buffer according to claim 9 further comprising a register for providing said bits which identify a thread number.

14. A translation look aside buffer for identifying real addresses of data stored in a memory for a plurality of threads being executed by a multi-thread CPU comprising:

an array of storage elements which caches address translation key value pairs;

a search engine for searching said array of memory elements to locate a real address of a group of pages stored in memory which are identified by a virtual page address, and a thread implicit mode bit associated with said virtual address;

a first logic circuit connected to receive said thread implicit bit; and concatenating with higher order bits of said real address of said group of pages data bits representing a thread being processed by said multithread CPU when said thread implicit bit is set to a first value, and concatenating with said higher order bits of said real address of said group of pages lower order bits of said real address when said thread implicit bit is set to a second value; and

a second logic circuit for concatenating to an address produced by said first logic circuit a portion of said virtual page address.

15. The translation look aside buffer for identifying real addresses of data stored in a memory according to claim 14 wherein said virtual page address includes an effective address, and said portion of said virtual page address which is concatenated with the address produced by said first logic circuit are the lower order bits of said effective address.

16. The translation look aside buffer for identifying real addresses of data stored in said memory of claim 14 wherein said virtual page address includes a process identification number and an effective address.

17. The translation look aside buffer for identifying real addresses of data stored in said memory of claim 16 wherein said second logic circuit concatenates the lower order bits of said effective address with the address produced by said first logic circuit.